

What Is Claimed Is:

- 1 1. A video compression system, comprising:
- 2 a processor-based platform coupled to a bus subsystem; and
- 3 coupled to the bus subsystem, a front end subsystem having at least a
- 4 DCT/IDCT module coupled to a motion estimation and
- 5 compensation engine (MEC engine) and to a quantizer/inverse-
- 6 quantizer (Q/Q^{-1}) module.
- 1 2. The video compression system according to Claim 1, wherein the DCT/IDCT
- 2 module includes:
- 3 a plurality of cores, each of said cores accepting input data and each of
- 4 said cores generating output data; and
- 5 a sequence generator receiving control signals from the bus subsystem and
- 6 in response thereto generating a plurality of control signals for
- 7 each of said cores.
- 1 3. The video compression system according to Claim 2, wherein the plurality of
- 2 cores comprises eight cores.

1 4. The video compression system according to Claim 2, wherein the plurality of
2 cores comprises four types of cores.

1 5. The video compression system according to Claim 4, wherein a first type of
2 core includes a main register for storing the input data and feedback data.

1 6. The video compression system according to Claim 4, wherein a second type of
2 core includes a first pair of lookup tables, and a third type of core includes a second pair
3 of lookup tables.

1 7. The video compression system according to Claim 6, wherein the second and
2 third types of cores each includes a temporary buffer, and the first and second pairs of
3 lookup tables each includes a 16-bit lookup table and a 12-bit lookup table.

1 8. The video compression system according to Claim 7, wherein the first pair of
2 lookup tables are selected to provide partial pixel values according to

3
$$V_i = A_3c + A_22^{-4}c + b,$$

4 wherein V_i represents an intermediate DCT value, A_3 and A_2 are 4-bit binary numbers, c
5 is a constant cosine coefficient, and b is a common coefficient.

1 9. The video compression system according to Claim 8, wherein the V_i is stored
2 in the temporary buffer for further DCT processing.

1 17. A DCT/IDCT circuit for enabling forward and inverse discrete cosine
2 transform of a datablock, comprising:
3 a plurality of cores, each having input data and output data, wherein the
4 input data for each core includes external data and output data
5 feedback from selected ones of the cores.

1 18. The DCT/IDCT circuit according to Claim 17, further comprising:
2 a sequence generator coupled to each core.

1 19. The DCT/IDCT circuit according to Claim 17, wherein the selected ones of
2 the cores comprises four cores.

1 20. The DCT/IDCT circuit according to Claim 17, wherein the external data
2 comprises the datablock, the datablock including prediction data processed by an MEC
3 engine communicatively coupled to the DCT/IDCT circuit.

1 21. The DCT/IDCT circuit according to Claim 17, wherein the external data
2 comprises the datablock, the datablock including reconstruction data processed by an
3 inverse quantizer module communicatively coupled to the DCT/IDCT circuit.

1 22. The DCT/IDCT circuit according to Claim 17, wherein the plurality of cores
2 comprises 8 cores.

1 23. The DCT/IDCT circuit according to Claim 17, wherein the

2 plurality of cores comprises four types of cores.

1 24. The DCT/IDCT circuit according to Claim 23, wherein a first type of core
2 includes a main register for storing the input data and feedback data.

1 25. The DCT/IDCT circuit according to Claim 23, wherein a second type of core
2 includes a first pair of lookup tables, and a third type of core includes a second pair of
3 lookup tables.

1 26. The DCT/IDCT circuit according to Claim 23, wherein a fourth type of core
2 includes two pairs of lookup tables.

1 27. A DCT circuit enabling forward discrete cosine transform of a datablock,
2 comprising:

3 a plurality of cores, each having input data and output data, wherein the
4 input data for each core includes external data and output data
5 feedback from selected ones of the cores.

1 28. The DCT circuit according to Claim 27, further comprising:
2 a sequence generator coupled to each core.

1 29. The DCT circuit according to Claim 27, wherein the selected ones of the
2 cores comprises four cores.

3 30. An IDCT circuit enabling inverse discrete cosine transform of a datablock,
4 comprising:

5 a plurality of cores, each having input data and output data, wherein the
6 input data for each core includes external data and output data
7 feedback from selected ones of the cores.

1 31. The IDCT circuit according to Claim 30, further comprising:
2 a sequence generator coupled to each core.

1 32. The IDCT circuit according to Claim 30, wherein the selected ones of the
2 cores comprises four cores.

1 33. A video processing system, comprising:
2 a processor-based platform coupled to a bus subsystem; and
3 coupled to the bus subsystem, a front end subsystem having at least a
4 circuit including
5 a plurality of cores, each of said cores accepting input data and
6 each of said cores generating output data; and
7 a sequence generator receiving control signals from the bus
8 subsystem and in response thereto generating a plurality of
9 control signals for each of said cores.

1 34. The video processing system according to Claim 33, further comprising:

2 a motion estimation and compensation engine and a quantizer/inverse-
3 quantizer (Q/Q-1) module both communicatively coupled to the
4 circuit.

1 35. The video processing system according to Claim 33, wherein the input data
2 for each core includes external data and output data feedback from selected ones of the
3 cores remaining.

1 36. The video processing system according to Claim 35, wherein the plurality of
2 cores comprises eight cores.

1 37. The video processing system according to Claim 33, wherein the circuit
2 comprises one of a DCT circuit, an IDCT circuit, and a DCT/IDCT circuit

1 38. A DCT/IDCT circuit for enabling forward and inverse discrete cosine
2 transform of a datablock, comprising:

3 means for selecting one of input data of the datablock received and a sum
4 of said input data and feedback data in order to provide first output
5 data;

6 coupled to the means for selecting, means for determining first partial
7 products based on the input data, the first output data and the
8 feedback data;

9 coupled to the means for selecting and the means for determining first

10 partial products, means for determining an intermediate result
11 based on a sum of the first partial products; and
12 coupled to the means for selecting, the means for determining first partial
13 products, and the means for determining an intermediate result,
14 means for providing the intermediate result as an operand added to
15 second partial products to obtain a final result.

1 39. The DCT/IDCT circuit according to Claim 38, further including means for
2 obtaining the final result within two clock cycles.

40. A DCT/IDCT circuit for enabling forward and inverse discrete cosine transform of a datablock, comprising:

- means for receiving input data associated with the datablock;
- coupled to the means for receiving, first means for selecting one of the input data and a sum of the input data and feedback data to provide first output data;
- coupled to the first means, second means for determining a sum of first partial products based on the input data, the feedback data, and first coefficient data to provide second output data;
- coupled to the means for receiving input data, third means for determining a sum of second partial products based on the input data, the feedback data, and second coefficient data to provide third output data;

